first gates of said plural numbers of said semiconductor memory cells, which are connected to the same data line at said drain regions thereof, are connected with word lines, being different from each other.

REMARKS

Examination is requested.

Respectfully submitted,

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MARKED UP VERSION OF REWRITTEN CLAIMS

10. (Amended) A semiconductor memory cell in a memory cell array, comprising:

the semiconductor memory cells as defined in [either on of the] claim[s] 5 [to 9], being aligned in plural numbers thereof, wherein they are driven by a data line and word line, wherein:

drain regions of plural numbers of semiconductor memory cells are connected to a same data line;

second gates of said plural numbers of said semiconductor memory cells, which are connected to the same data line at said drain regions thereof, are connected with each other; and

first gates of said plural numbers of said semiconductor memory cells, which are connected to the same data line at said drain regions thereof, are connected with word lines, being different from each other.